In the Claims:

1. – 13. (canceled)

14. (currently amended) A lamination ~~multiplayer~~ multilayer substrate, at least comprising:

a plurality of laminating layers stacked and laminated together, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of first vias with a first ends and second ends positioned within the dielectric layer, wherein the first ends of the first vias electrically connect with the patterned conductive layer and the second ends of the first vias electrically connect with an adjacent said laminating layer and a barrier metal layer between said first vias and said patterned conductive layer, wherein said barrier metal layer is a stop layer to form said first vias and said patterned conductive layer; and

a bottom layer stacked and laminated with the plurality of laminating layers and disposed at a bottom side of the ~~multiplayer~~ multilayer substrate, wherein said bottom layer has a second dielectric layer and a plurality of second vias penetrating the second dielectric layer and electrically connecting with the plurality of laminating layers, wherein said first dielectric layers and said second dielectric layer are bonded together.

15. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 14, further comprising two pad opening layers disposed respectively at top and bottom sides of the ~~multiplayer~~ multilayer substrate.

16. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 15, wherein said pad opening layer is a solder mask.

17. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 14, further comprising a metal layer disposed ~~on~~ between said second ends of the vias and one of said adjacent laminating layer and said core substrate.

18. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 17, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

19. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 14, further comprising a heat sink disposed a top side of said ~~multiplayer~~ multilayer substrate.

20. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 14, wherein said first and said second dielectric layers are selected from one of a thermal plastic resin and a thermal setting resin.

21. (currently amended) A lamination ~~multiplayer~~ multilayer substrate, at least comprising:

a core substrate having a plurality of through holes therein; and

a plurality of laminating layers stacked and laminated with said core substrate, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of vias with a first ends and second ends positioned within the dielectric layer and a barrier metal layer between the patterned conductive layer and the vias, wherein the barrier metal layer is a stop layer to form the patterned conductive layer and the vias and the first ends of the vias electrically connect with the patterned conductive layer and the second ends of the first vias electrically connect with one of an said adjacent said laminating layer and said core substrate, wherein said first dielectric layers are bonded together.

22. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, further comprising two pad opening layers disposed respectively at top and bottom sides of the ~~multiplayer~~ multilayer substrate.

23. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 22, wherein said pad opening layer is a solder mask.

24. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, further comprising a metal layer disposed ~~on~~ between said second ends of the vias and one of said adjacent laminating layer and said core substrate.

25. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 24, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

26. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, further comprising a heat sink disposed a top side of said ~~multiplayer~~ multilayer substrate.

27. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, wherein said first dielectric layers are selected from one of a thermal plastic resin and a thermal setting resin.

28. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, wherein said laminating layers are laminated on both two sides of said core substrate.

29. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, wherein said laminating layers are laminated on one side of said core substrate.

30. (currently amended) The ~~multiplayer~~ multilayer substrate according to claim 21, further comprising a heat sink disposed a top side of said ~~multiplayer~~ multilayer substrate.

31. (new) A laminating layer of a lamination multilayer substrate, at least comprising:

a first dielectric layer;

a circuit metal layer within and between said first dielectric layer;

a barrier metal layer on said circuit metal layer;

a plurality of vias on said barrier metal layer; and

a second dielectric layer on said circuit metal layer, said first dielectric layer, said barrier metal layer and between said vias.

32. (new) The laminating layer of a lamination multilayer substrate according to claim 31, wherein said first dielectric layer comprises a semi-cured material.

33. (new) The laminating layer of a lamination multilayer substrate according to claim 31, wherein said circuit metal layer and said vias comprise a copper layer and copper vias.

34. (new) The laminating layer of a lamination multilayer substrate according to claim 31, wherein said barrier metal layer is selected from one of chrome, lead, aluminum, silver, nickel, tin, lead and tin lead alloy.

35. (new) The laminating layer of a lamination multilayer substrate according to claim 31, wherein said second dielectric layer is selected from one of a thermal plastic resin and a

thermal setting resin.